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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,361	03/29/2001	Noriaki Sakamoto	10417-074001	3784

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EXAMINER

CHU, CHRIS C

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 12/21/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/821,361

Applicant(s)

SAKAMOTO ET AL.

Examiner

Chris C. Chu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 November 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 - 12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 March 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Response to Election

1. Applicant's election of Group I in Paper No. 4 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Drawings

2. Figure 12 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "70" and "71" have been used to designate both chip and bridge. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

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4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "4" and "12" have both been used to designate first die pad. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: reference characters "56C" in Fig. 3A, "59A" in Fig. 4A, "59B" in Fig. 4A, "60A" in Fig. 4A, and "11" in Fig. 12 are not referenced in the specification of instant invention. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

6. The drawings are objected to because reference numbers "81" in Fig. 7 and "80" in Fig. 11 are not pointing correct structure in the figures. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

7. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: the reference character "O" in the specification is not referenced in the figures. A proposed drawing

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correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

8. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first and second semiconductor chip which are superposed on each other, at least one bridge arranged between said first and second semiconductor chip, and the insulating resin exposes the rear surface of each of said bridge must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

9. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Specification

10. The disclosure is objected to because of the following informalities:

Abstract, line 3, erase some extra spaces before "they."

The specification needs an extra line before sub-titles.

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On pages 2 and 15, removes "..."

On page 2, line 15, needs a space before 7.

On page 6, lines 26 and 28, "the bonding pad" should be --a bonding pad--.

On page 11, line 12, removes some extra space between "the" and "external."

On page 13, line 12, removes some extra space between "the" and "asemiconductor."

On page 19, line 7, removes some extra space before "a."

The specification does not have a brief description of the Figs. 1A – 1E, Figs. 2A – 2E, Figs. 3A – 3E, and Figs. 4A – 4E. Also, the brief descriptions of each figure are not clearly describing the drawings and contain some errors such as Fig. 1 ~ 6 are a view of a "first" semiconductor device.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 10 ~ 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 10, it can not be determined what the applicant regards as the "first and second semiconductor chip which are superposed on each other, at least one bridge arranged between said first and second semiconductor chip, and the insulating resin exposes the rear surface of each

of said bridge". Further, the arrangement of the bridge in the claimed structure is not clear.

Therefore, the arrangement of the bridge in the claimed structure must be clearly defined in the specification or the claim cancelled from instant invention. No new matter should be entered.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1 ~ 6 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ugon.

Note Figs. 6 and 7 of Ugon, where he/she shows a semiconductor device comprising: a first (43) and a second (44) semiconductor chip which are electrically connected to each other (see Fig. 6); a bridge (47b) arranged between said first and said second semiconductor chip and electrically connecting them (see Fig. 6); external connecting electrodes (48a and 48c) provided to surround areas where said first and said second semiconductor chip are located, at least a portion of the rear surface of them serving as an electrode to be externally connected (see Figs. 6 and 7); first metallic wires (46) which electrically connect said first and said second semiconductor chip to said external connecting electrodes, respectively (see Figs. 6 and 7); second metallic wires (46 in middle) which electrically connect said first and said second semiconductor chip to said bridge (see Figs. 6 and 7); and insulating resin (49) which seals said first and said second semiconductor chip, said external connecting electrodes, and said first and

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said second metallic wires (see Fig. 7), wherein said insulating resin (49) exposes the rear surface of each of said bridge and said external connecting electrodes (see Fig. 7), and said second metallic wires are ball-bonded on said first and said second semiconductor chip and stitch-bonded on said bridge. Further, since Ugon does not limit the sealing material to any particular or specific sealing material, his/her disclosure encompasses all well known sealing material including "resin." Even further, the phrase "said second metallic wires are ball-bonded on said first and said second semiconductor chip and stitch-bonded on said bridge" is a method of forming a device, which is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight.

Regarding claims 2 and 5, Ugon discloses the rear surface of each of said insulating resin and said badge is coated with an insulating film (42 in Fig. 7 and column 7, lines 35 ~ 37).

Regarding claims 3 and 6, note Fig. 7 of Ugon, where he/she shows the rear surface of each of said insulating resin, said bridge and said external connecting electrodes is coated with an insulating film (42 in Fig. 7 and column 7, lines 35 ~ 37) so that said external connecting electrodes are partially exposed (see Fig. 7).

Regarding claim 4, note Fig. 7 of Ugon, where he/she shows a semiconductor device comprising: a first (43) and a second (44) semiconductor chip which are electrically connected to each other (see Figs. 6 and 7); a first die pad (47a, the left) to which said first semiconductor chip is fixed (see Figs. 6 and 7); a second die pad (47a, the right) to which said second semiconductor chip is fixed (see Figs. 6 and 7); at least one bridge (47b) arranged between said first and said second semiconductor chip and electrically connecting them (see Figs. 6 and 7); external connecting electrodes (48a and 48c) provided to surround areas where said first and said second

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semiconductor chip are located, at least a portion of the rear surface of them serving as an electrode to be externally connected (see Figs. 6 and 7); first metallic wires (46) which electrically connect said first and said second semiconductor chip to said external connecting electrodes, respectively (see Figs. 6 and 7); second metallic wires (46 in middle) which electrically connect said first semiconductor chip, said bridge and said second semiconductor chip (see Figs. 6 and 7); and insulating resin (49) which seals said first and said second semiconductor chip, said external connecting electrode, and said first and said second metallic wires (see Fig. 7), wherein said insulating resin (49) exposes the rear surface of each of said bridge and said external connecting electrodes (see Fig. 7), and said second metallic wires are ball-bonded on said first and said second semiconductor chip and stitch-bonded on said bridge. Further, since Ugon does not limit the sealing material to any particular or specific sealing material, his/her disclosure encompasses all well known sealing material including "resin." Even further, the phrase "said second metallic wires are ball-bonded on said first and said second semiconductor chip and stitch-bonded on said bridge" is a method of forming a device, which is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight.

Regarding claim 12, note Fig. 7 of Ugon, where he/she shows the rear surface of each of said insulating resin, said first and said second die pad, said bridge and said external connecting electrodes is coated with an insulating film (42 in Fig. 7 and column 7, lines 35 ~ 37) so that said first die pad, said second die pad and/or said external connecting electrodes are partially exposed (see Fig. 7).

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15. Claims 1 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al.

Regarding claims 1 and 4, note Fig. 3 of Lin et al., where he/she shows a semiconductor device comprising: a first (17) and a second (15) semiconductor chip which are electrically connected to each other (see Fig. 3); a first die pad (19, the left) to which said first semiconductor chip is fixed (see Fig. 3); a second die pad (19, the right) to which said second semiconductor chip is fixed (see Fig. 3); at least one bridge (13, the middle) arranged between said first and said second semiconductor chip and electrically connecting them (see Fig. 3); external connecting electrodes (13) provided to surround areas where said first and said second semiconductor chip are located, at least a portion of the rear surface of them serving as an electrode to be externally connected (see Fig. 3); first metallic wires (18) which electrically connect said first and said second semiconductor chip to said external connecting electrodes, respectively (see Fig. 3); second metallic wires (18 in middle) which electrically connect said first semiconductor chip, said bridge and said second semiconductor chip (see Fig. 3); and insulating resin (20) which seals said first and said second semiconductor chip, said external connecting electrode, and said first and said second metallic wires (see Fig. 3), wherein said insulating resin (20) exposes the rear surface of each of said bridge and said external connecting electrodes (see Fig. 3), and said second metallic wires are ball-bonded on said first and said second semiconductor chip and stitch-bonded on said bridge. Further, the phrase “said second metallic wires are ball-bonded on said first and said second semiconductor chip and stitch-bonded on said bridge” is a method of forming a device, which is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight.

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16. Claims 7 ~ 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Fukui et al.

Note Figs. 7(a) and 1 of Fukui et al., where he/she shows a semiconductor device comprising: a first (1) and a second (2) semiconductor chip which are superposed on each other (see Fig. 7(a)); a bridge (4, the left) electrically connecting said first and said second semiconductor chip (see Fig. 7(a)); external connecting electrodes (4) provided to surround areas where said first and said second semiconductor chip are located, at least a portion of the rear surface of them serving as an electrode to be externally connected (see Figs. 7(a) and 2(g)); first metallic wires (8) which electrically connect said first and said second semiconductor chip to said external connecting electrodes, respectively (see Fig. 7(a)); second metallic wires (8 on top of 4, the left) which electrically connect said first and said second semiconductor chip to said bridge (see Fig. 7(a)); and insulating resin (9) which seals said first and said second semiconductor chip, said external connecting electrode, and said first and said second metallic wires (see Fig. 1), wherein said insulating resin (9) exposes the rear surface of each of said bridge and said external connecting electrodes (see Fig. 1), and said second metallic wires are ball-bonded on said first and said second semiconductor chip and stitch bonded on said bridge. Further, the phrase “said second metallic wires are ball-bonded on said first and said second semiconductor chip and stitch-bonded on said bridge” is a method of forming a device, which is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight.

Regarding claim 8, Fukui et al. discloses the rear surface of each of said insulating resin and said bridge is coated with an insulating film (3 in Fig. 1).

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Regarding claim 9, Fukui et al. discloses the rear surface of each of said insulating resin, said bridge and said external connecting electrodes is coated with an insulating film (3 in Fig. 1) so that said external connecting electrodes are partially exposed (see Fig. 1).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

18. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goto in view of Fukase et al.

Goto discloses the claimed invention except for an insulating resin for sealing said first and said second semiconductor chip, said external connecting electrode, and said first and said second metallic wires, wherein said insulating resin exposes the rear surface of each of said bridge and said external connecting electrodes; and an insulating film for coating the rear surface of each of said insulating resin, said first die pad and said bridge. However, Fukase et al. discloses an insulating resin (24 in Fig. 1(e)) for sealing said first and said second semiconductor chip, said external connecting electrode, and said first and said second metallic wires, wherein said insulating resin exposes the rear surface of each of said bridge and said external connecting electrodes (see Fig. 1(e)); and an insulating film (10 in Fig. 1(e)) for coating the rear surface of each of said insulating resin, said first die pad and said bridge (see Fig. 1(e)). Thus, it would have

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been obvious to one of ordinary skill in the art at the time when the invention was made to modify Goto by including the insulating resin and the insulating film as taught by Fukase et al. The ordinary artisan would have been motivated to modify Goto in the manner described above for at least the purpose of increasing reliability of the package. Further, the phrase "said second metallic wires are ball-bonded on said first and said second semiconductor chip and stitch-bonded on said bridge" is a method of forming a device, which is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight.

Regarding claim 11, Goto, as modified, discloses the rear surface of each of said insulating resin, said first die pad and said bridge is coated with an insulating film (3 in Fig. 1).

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Huang et al., Nakamura, Spielberger et al., Weinberg et al., Tang et al., Han et al., Sasaki, Hobson, and Kweon et al. disclose a semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the

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organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
December 17, 2001

A handwritten signature in black ink, appearing to read 'Eddie Lee', with a stylized, flowing script.

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800